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Shree Damodar College of Commerce & Economics, Margao-Goa
FY BCA Semester-I Semester End Examination, Nov 2022
Computer Organization and Architecture (CAC-102)

Duration: 2 Hours **Max Marks: 60**

Instructions: i) All Questions are compulsory
ii) Figures to the right indicate full marks

Q1.A) State TRUE or FALSE **(5x1=05)**

i) Once the cache has been filled, when a new block is brought into the cache, one of the existing blocks must be replaced

ii) The fetch cycle occurs at the end of each instruction cycle and causes an instruction to be fetched from memory

iii) Memory Buffer Register (MBR): Contains a word to be stored in memory, or is used to receive a word from memory

vi) DRAM doesn't Requires periodic charge refreshing to maintain data storage

v) Interrupts are provided primarily as a way to improve processing efficiency

Q1.B) Define the purpose of the following in not more than 20 words. **(5x1=05)**

i) Double Data Rate SDRAM
ii) Associative mapping
iii) Microinstruction execution
vi) Central Processing Unit(CPU)
v) Instruction Buffer Register (IBR)

Q.2 Answer the following

a) Explain the meaning of micro operations (2)

b) Explain 3 replacement algorithms used in memory cache. (3)

c) With the help of a diagram, explain the 3 alternative DMA configurations. (5)

Q3. Answer the following:

a) Explain the working of parallel and serial I/0 (2)

b) List and describe the three techniques that are possible for I/O operations. (3)

c) With the help of a diagram, explain any 3 addressing modes in detail. (5)

Q4. Answer the following:

a) Perform the following conversions. (2)

i) Binary to decimal:	11101
ii) Hexadecimal to decimal	$(2B3)_{16}$

b) With a help of a diagram explain sequential interrupts. (3)

c) Describe the working of any 3 RAID levels and justify its need. (5)

Q5. Answer the following.

a) Describe the two concerns involve in design of microinstructions sequencing techniques. (2)

b) Explain Instruction pipelining and stages. (3)

c) Describe the 4 general categories of techniques that are in common use for device identification. (5)

Q6. Answer the following.

a) Explain the working of control bus in brief (2)

b) With a help of a diagram, explain the fetch cycle. (3)

c) Describe 5 elements of instruction in detail. (5)

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